23.6 A 700/900mW/Channel CMOS Dual Analog Front-End IC for VDSL with Integrated 11.5/ 14.5dBm Line Drivers

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A dual channel IC for high-speed digital subscriber line (VDSL) provides the analog functions required for receiving and transmitting up to 52Mb/s, according to ETSI TS 101 270-2 V1.1.1 and ANSI T1E1.4/2000- 009R3. With an effective Bandwidth (BW) of 12MHz and with maximum voltage supply of 5V +/-5% and 2.5V +/-5% for the logic blocks, at least 30% lower power reduction over existing solutions [1] is achieved using a complete integration including two built in differential line drivers (LD).

Unlike previously reported VDSL circuits that use separate line drivers implemented with either BiCMOS or greater than 15V power supplies [1-3], this VDSL circuit completes the integration of the line driver in 5V CMOS. Additionally the core of the receiver contains an oversampled multibit continuous time Sigma-Delta Analog to Digital Converter (ΣΔ ADC). With this architecture, as with the logic blocks, the converter supply is also reduced to 2.5V allowing further reduction of power.

The two port device is intended for use in the central office (CO). A single channel for dedicated customer premises equipment (CPE) also allows usage in remote applications.

The two Analog Front Ends (AFE) are shown in Fig. 23.6.1. Both channels consists of a DAC, post filter, and a line driver on the transmit side. The receive side contains a variable gain amplifier (VGA), a pre filter, and an ADC. The ADC is followed by subsequent decimation stages. The multibit output of the modulator passes through a SINC4/4 and a programmable 7th order IIR-filter. This filter delivers a 14b wide 60MHz output stream.

Both channels operate almost independently of each other. Common blocks, like the shared data I/O interface, PLL and serial bus interface are used to reduce the overall pin count and allow the necessary board space for routing.

The Digital-to-Analog Converter (DAC) consists of three blocks: an interpolation filter, current steering DAC, and a 3rd order post filter. The interpolation filter receives a 14b data stream in two's complement at 15 or 30MS/s depending on the chosen operating mode. It has an up sampled output of 120MS/s which feeds the current steering DAC. The RC continuous-time post filter following the DAC guarantees the required suppression of all out-of-band images and noise.

Integrating the line driver at low voltage conflicts with the need for low power because it implies a high transformer ratio of 1:4. The 14.5dBm line power translates to 600mA peak currents. This current peak is supplied by the line driver. To reduce the power consumption the line driver idle current is set to 1/50 of the peak current. Along with high operating frequencies these requirements pose a real challenge in line driver design. The low idle current limits the LD class AB output stage to about 8dB signal-to-distortion (S/D)

To achieve 75dB S/D, the LD must have a loop gain of at least 67dB at 11MHz. An operational amplifier (opamp) designed with a single pole roll-off would need a unity-gain bandwidth (UGBW) of more than 24GHz. Even a multi-path opamp design with 60dB/dec roll-off would require a UGBW of close to 1GHz, considering gain and phase margin requirements. Neither solution is possible using a 0.5μm CMOS technology. The LD reaches an ultimate linearity with lower UGBW by means of a sophisticated compensation technique. Because the scaled distortion components are presented on the inverting inputs, a Gm amplifier, similar to [5] is used. The dual-ended outputs of the Gm amplifier are fed to the inputs of the pair of second amplifiers. Since, the distortion components are out of phase they cancel each other. This is shown in Fig. 23.6.2.

Figure 23.6.2, lower portion, shows the Hybrid/VGA. The VGA allows the dynamic range of the received signal to be adapted to best fit the signal-to-noise ratio (SNR) and dynamic range requirements of the ΣΔ ADC.

Both the transmitter and receiver paths provide 13b performance. This allows for a simplified Hybrid/VGA cancellation circuit. To match the impedance, resistor RL is programmed using 3b to adjust for 30% of line impedance. The VGA consumes 135mW, with gain range of 0-35dB. Power is reduced by means of bypassing the second stage via path B to 90mW when lower gains, 0-23dB, are used. Measurement results at 4MHz input full scale, a third order harmonic distortion (H3) is below 79dB.

Due to the high transformer ratio, Rx noise sensitivity is increased. The Hybrid input referred noise needed is 5nV/√(Hz). The first attempt had 14nV/√(Hz) but a second attempt replacing the input 5V devices with 2.5V transistors and increasing the tail current from 1.6mA to 3.2mA achieves this specification.

Figure 23.6.3 shows the main core of the opamp. Using multi gain stages having 60dB/dec roll off up to 15MHz and 20dB/dec beyond. The high open-loop gain achieved with this method, at the VDSL BW, allows a class AB design with only 9mA. To make the common-mode (CM) loop fast, each amplifier has three CM loops. They are readily compensated and contribute a small amount to the overall distortion. Figure 23.6.4 shows the measurement results of the complete Hybrid and VGA

Figure 23.6.5 shows the continuous time multi bit 3rd order self-calibrating ΣΔ ADC block diagram. The analog modulator uses an over sampling ratio (OSR) of 10, resulting in a sampling frequency of 240MHz. To meet the low jitter requirements and high clock rate of this type a PLL is implemented and a 980MHz LC VCO is used to produce the needed low jitter and high clock rate.

With the VCO a phase noise of −105dBc at 100kHz offset, and PLL BW of 350kHz jitter is reduced below the ΣΔ ADC requirement of 12pS and allows the ΣΔ ADC to exceed 13b of performance at only 75mW.

Two on chip calibration loops are implemented. One, calibrates the offset of flash comparator in the ΣΔ ADC permitting the use of smaller input devices which provide lower input capacitance and a denser layout. The other calibrates the noise shaping variation of the converter. It sets the poles of the ΣΔ ADC to within 1-2% variations instead of 40% due to the on chip RC variations.

An extra loop provides delay adjustment to overcome the low OSR and the delay in the ΣΔ ADC loop which reduces the stability of the converter. The desired 79dB SNR is achieved when a 14.5dBm signal is applied. Figure 23.6.6 shows the results of laboratory measurements.

Cross-talk sensitivity is addressed using 1mm dead zone spacing between the 2 DSLs and keeping the transmitter power devices 7mm apart. For a 2MHz input signal Tx1 to Tx2 at the line output rejection was -90dB. Further improvements such as Deep N-well are avoided due to cost. Figure 23.6.7 shows a photo of the assembled chip utilizing a die size of 31mm² /channel. The VDSL chip is realized in 0.25/0.5μm CMOS. The solid lines covering the die are the metal density patterns.

Acknowledgements

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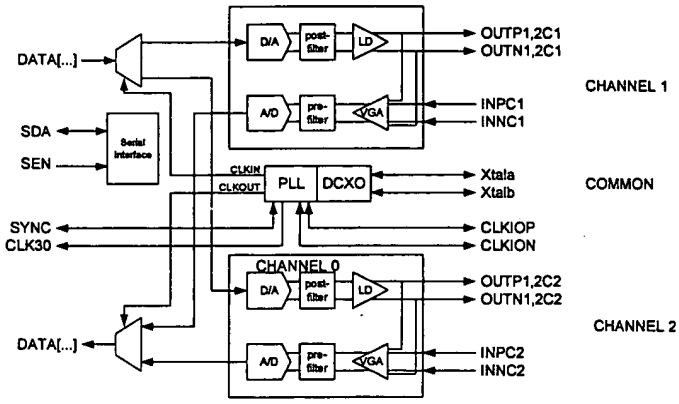

Figure 23.6.1: Overall block diagram.

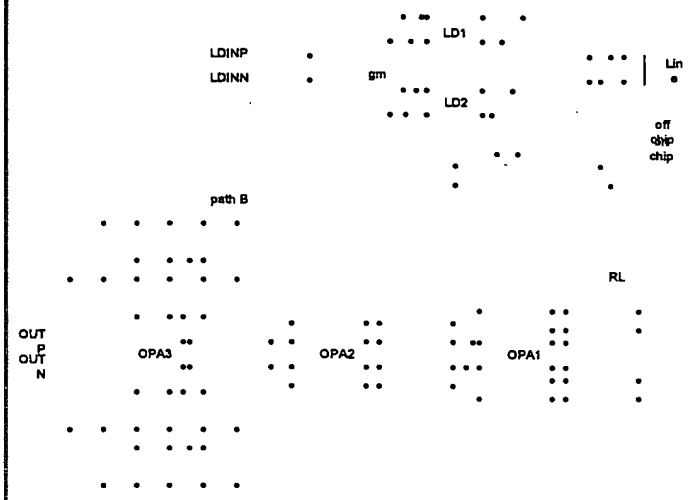

Figure 23.6.2: Line driver, VGA and Hybrid circuit diagram.

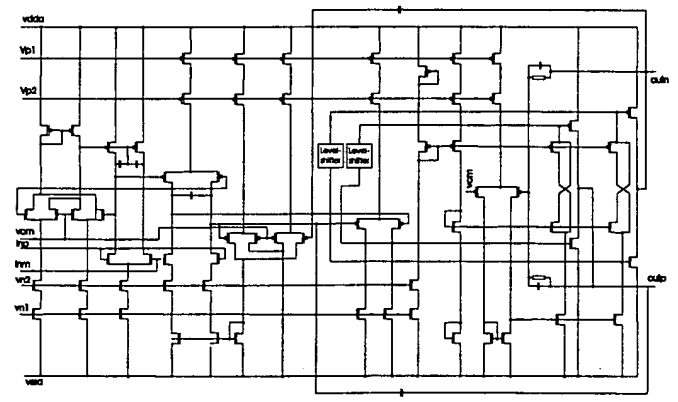

Figure 23.6.3: Core amplifier with its multi-loop common-mode circuit.

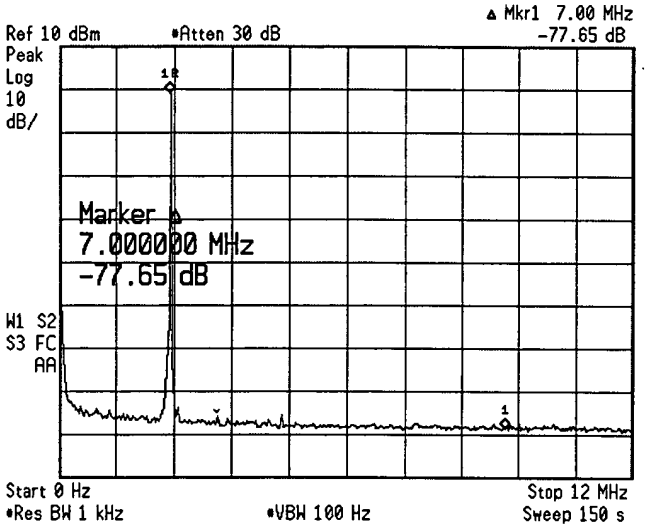

Figure 23.6.4: Measured spectrum of combined Hybrid and VGA.

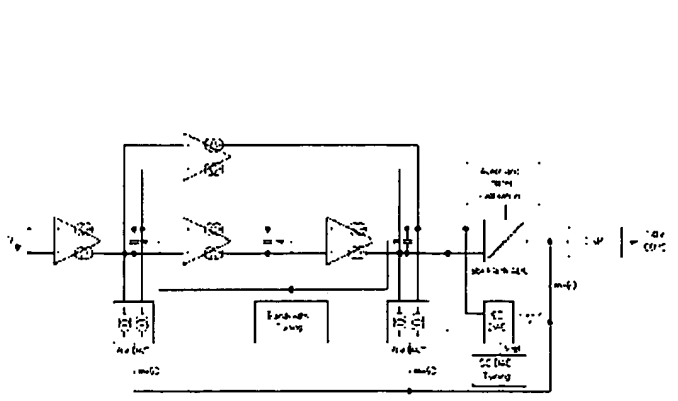

Figure 23.6.5: ΣΔ ADC architecture.

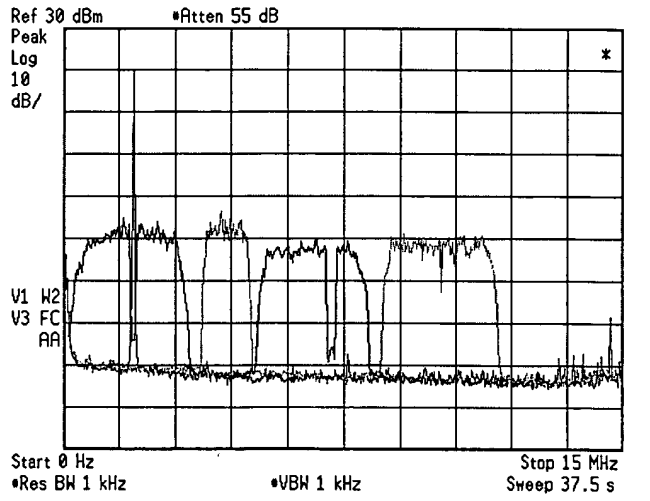

Figure 23.6.6: Measured transmitter response with a VDSL signal.

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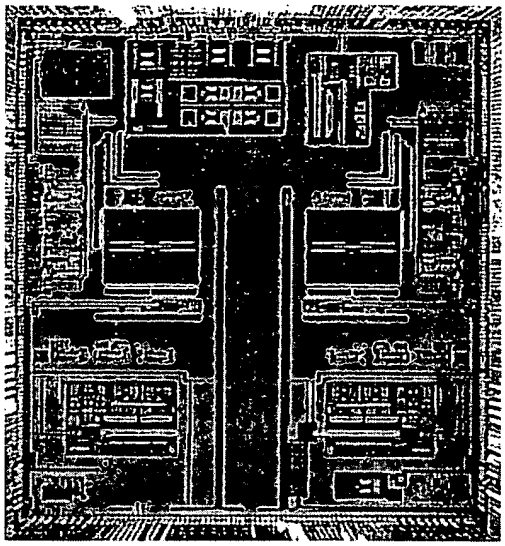

Figure 23.6.7: Assembled die micrograph.

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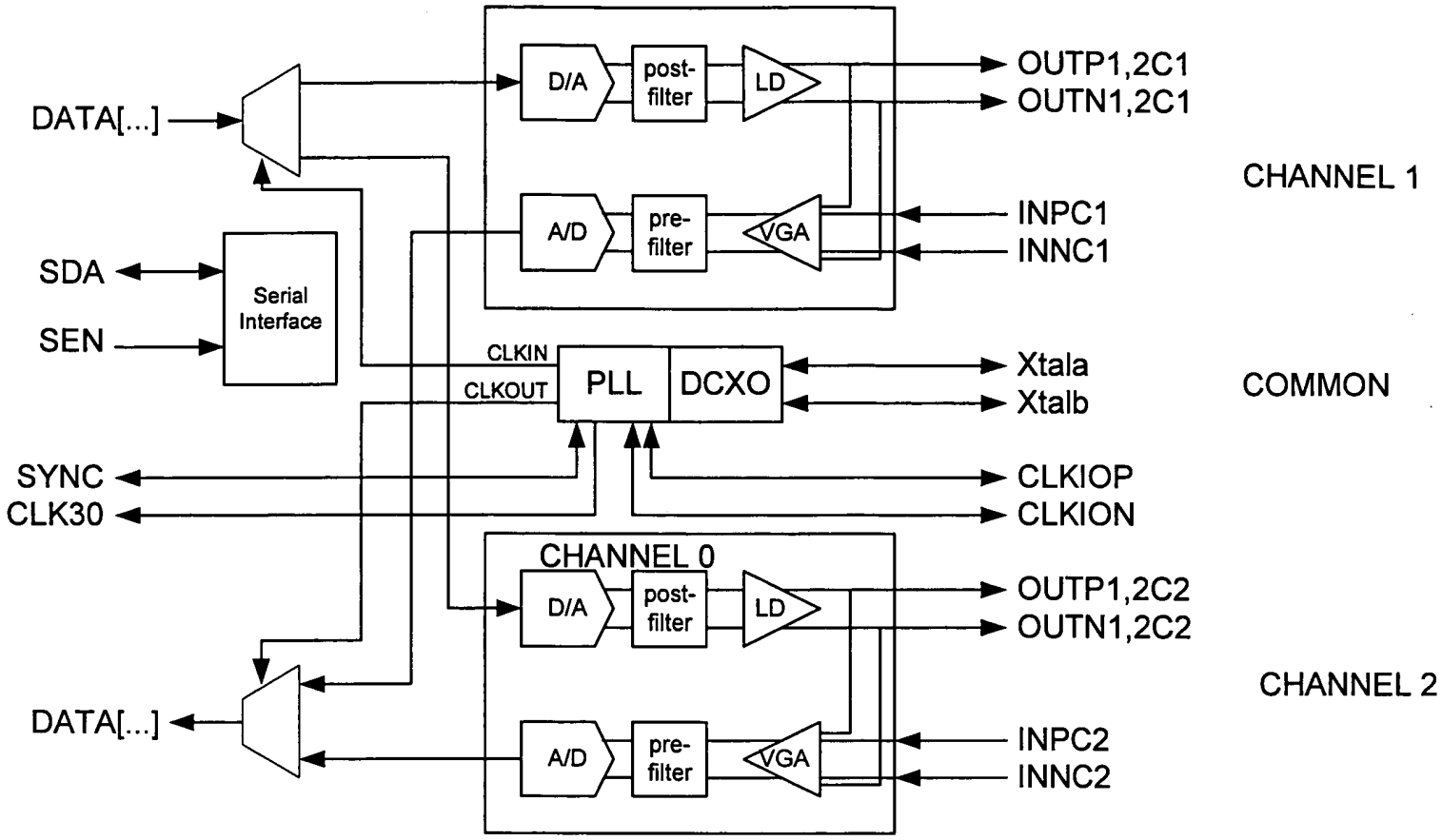

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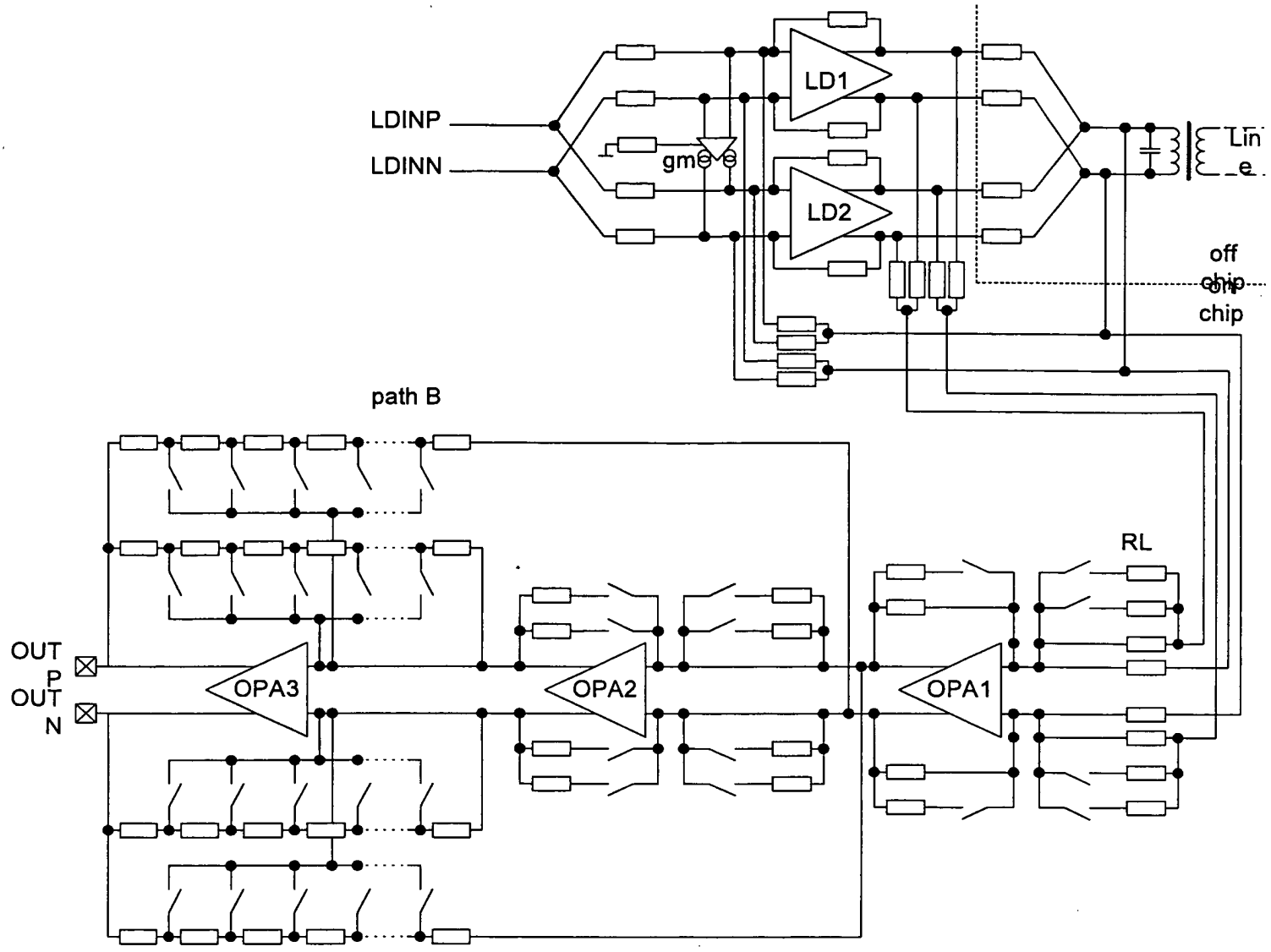

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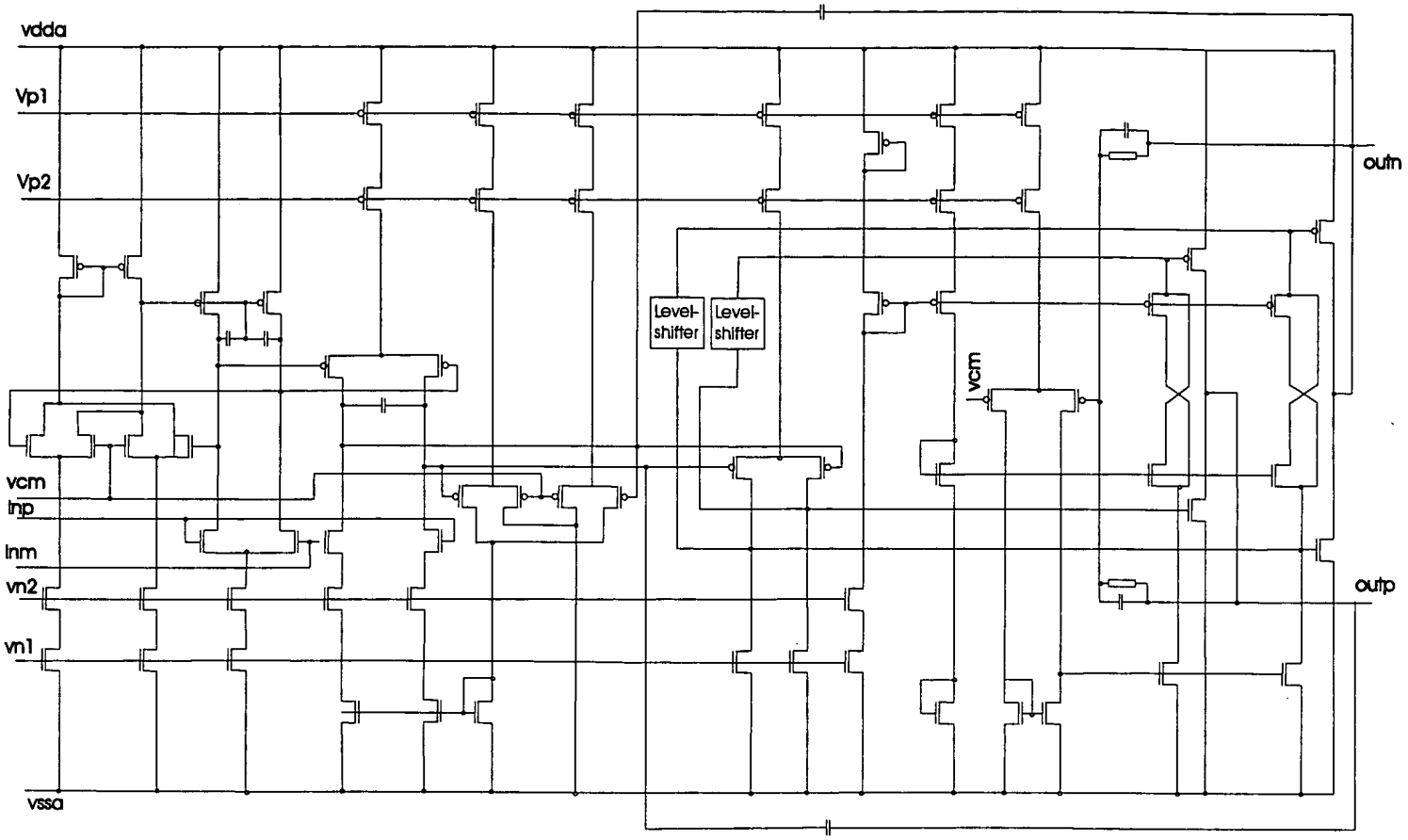

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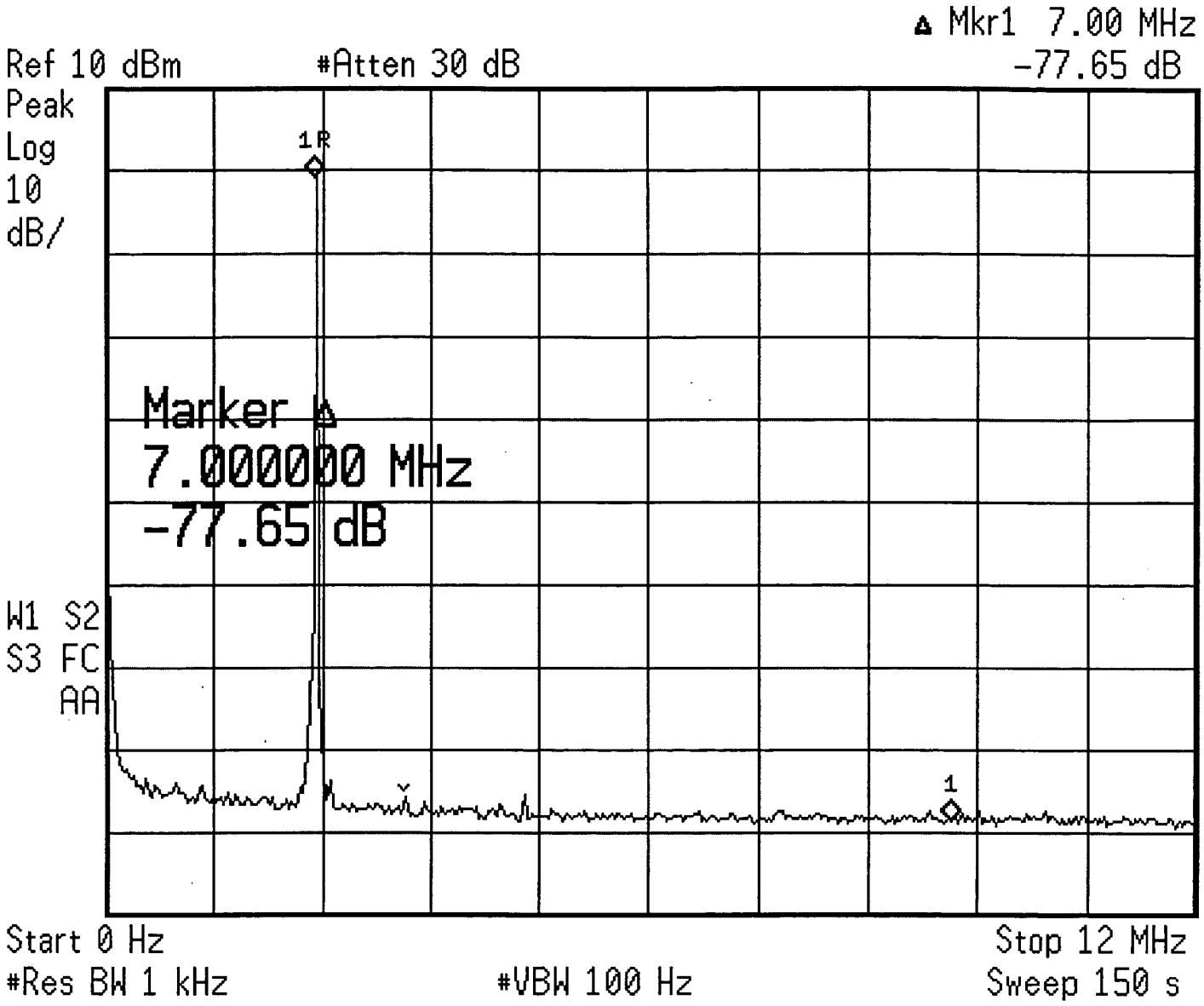

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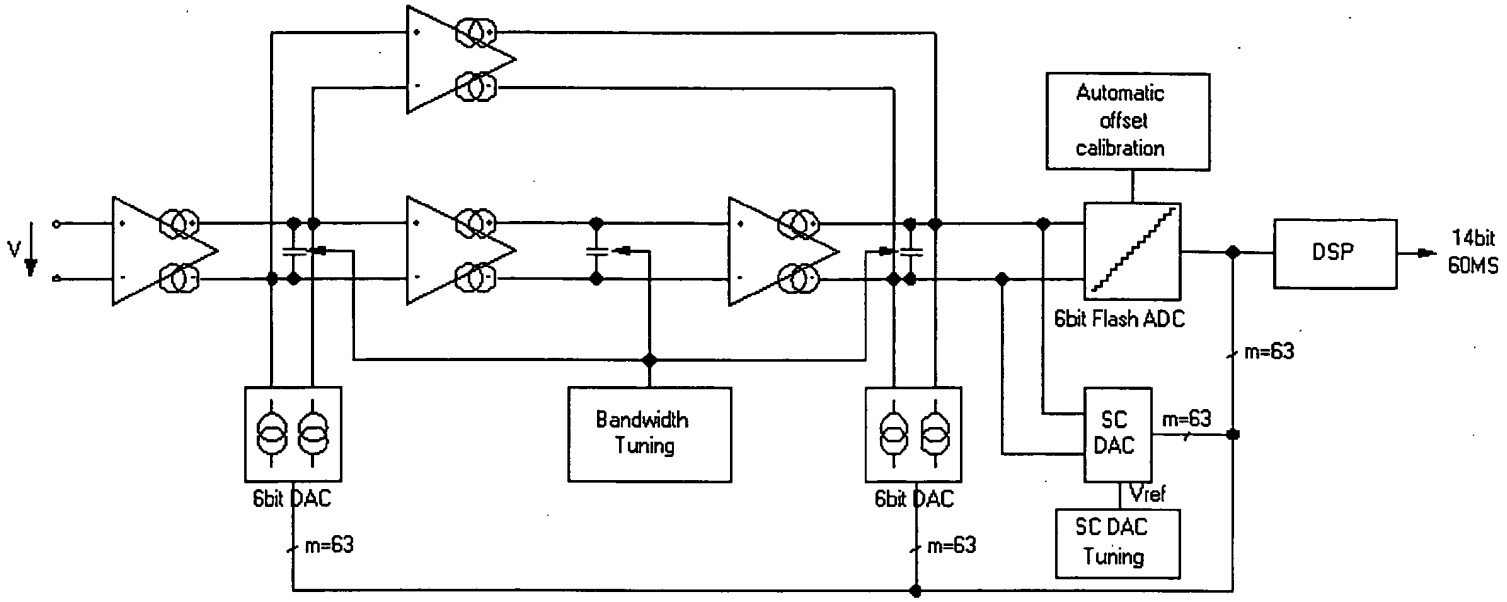

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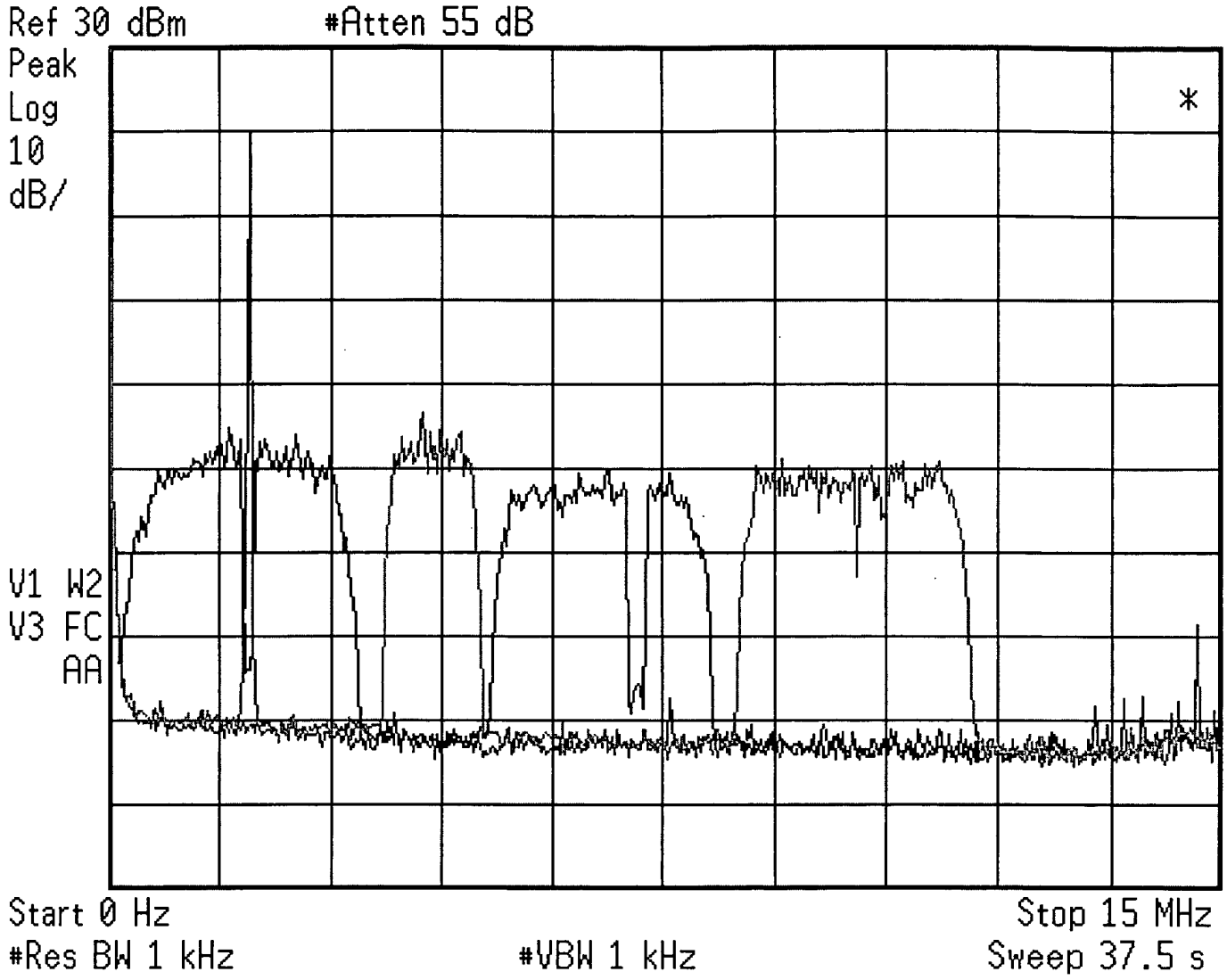

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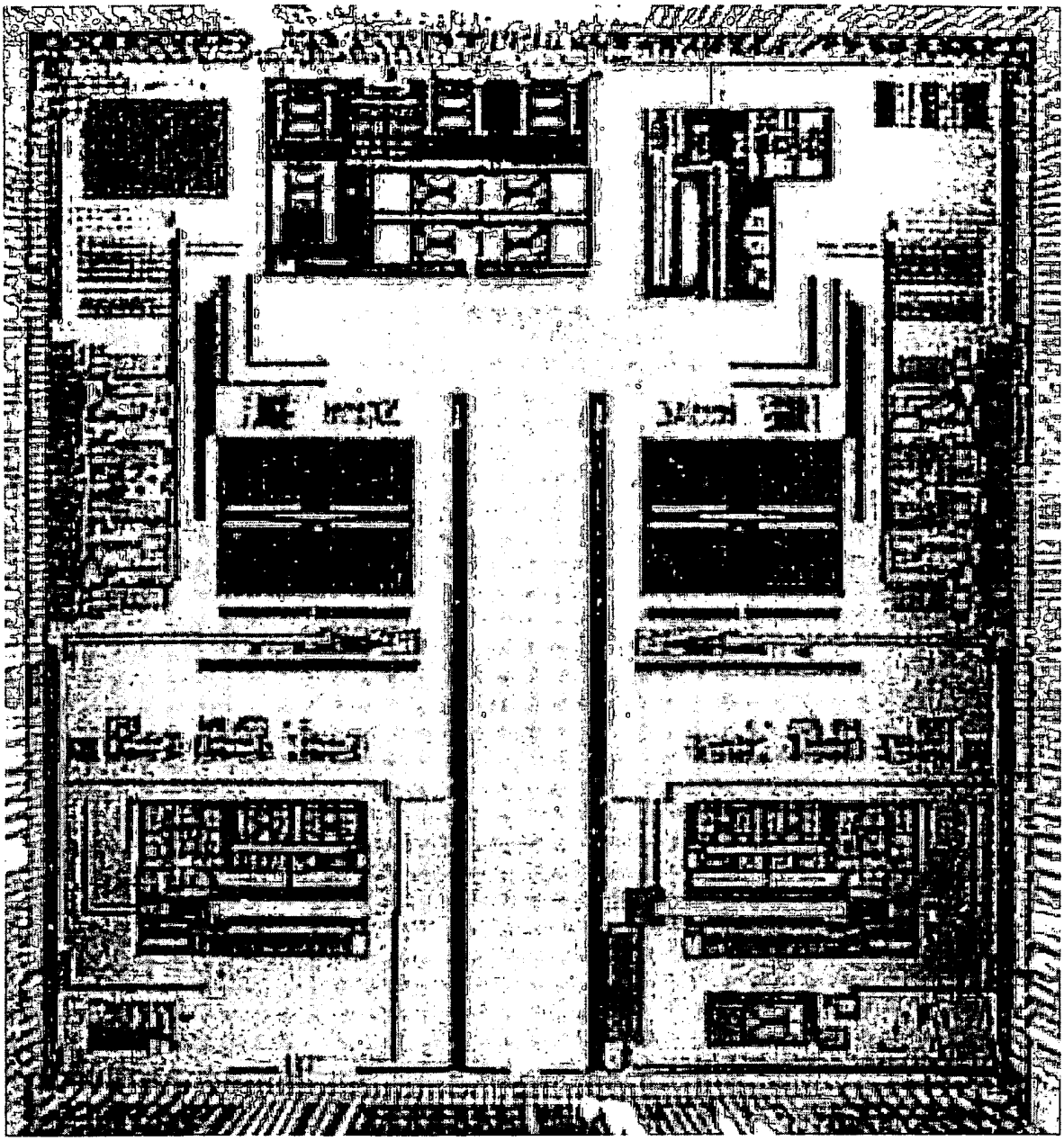

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